IN THE CLAIMS:

Please amend the claims as follows:

1-29. (Canceled)

30. (New) A digital data synchronization apparatus, comprising:

a first synchronization circuit for synchronizing a first frequency signal with a first received data signal and for generating a first comparison signal;

a second synchronization circuit for synchronizing a second frequency signal with a second received data signal and for generating a second comparison signal;

a first interconnection for transmitting the first comparison signal to the second synchronization circuit; and

a second interconnection for transmitting the second comparison signal to the first synchronization circuit,

the first synchronization circuit including a first corrector for adjusting the first frequency signal in response to the second comparison signal and

the second synchronization circuit including a second corrector for adjusting the second frequency signal in response to the first comparison signal.

31. (New) The digital-data synchronization apparatus according to claim 30, wherein the first frequency signal and the second frequency signal are derived from a common source that includes multiple components.

32. (New) The digital-data synchronization apparatus of claim 30, wherein at least one member selected from the group consisting of the first synchronization circuit and the second synchronization circuit includes a composite phase frequency detector including a phase frequency detector, a multiplier phase detector coupled to the phase frequency detector and a divide by two flip-flop coupled to both the phase frequency detector and the multiplier phase detector, the divide by two flip-flop conditioning a common input signal to both the phase frequency detector and the multiplier phase detector to a 50% duty cycle.

33. (New) The digital-data synchronization apparatus of claim 32, further comprising another divide by two flip-flop coupled to the phase frequency detector and a further divide by two flip flop coupled to the multiplier phase detector.

34. (New) The digital-data synchronization apparatus of claim 32, wherein the multiplier phase detector includes a logic gate.

35. (New) The digital-data synchronization apparatus of claim 34, wherein the logic gate includes an XOR gate.

36. (New) The digital-data synchronization apparatus of claim 30, wherein the first frequency signal and the second frequency signal are characterized by a known integer ratio of frequency, phase or both frequency and phase.

37. (New) A method of providing digital-data synchronization, comprising:

synchronizing a first frequency signal with a first received data signal and generating a first comparison signal using a first synchronization circuit;

synchronizing a second frequency signal with a second received data signal and generating a second comparison signal using a second synchronization circuit;

providing said first comparison signal to said second synchronization circuit;

providing said second comparison signal to said first synchronization circuit;

adjusting said first frequency signal in response to said second comparison signal; and

adjusting said second frequency signal in response to said first comparison signal.

38. (New) The method of claim 37, wherein at least one member selected from the group consisting of i) synchronizing the first frequency signal with the first received data signal and generating the first comparison signal using the first synchronization circuit and ii) synchronizing the second frequency signal with the second received data signal and generating the second comparison signal using the second synchronization circuit includes using a composite phase frequency detector including a phase frequency detector, a multiplier phase detector coupled to the phase frequency detector and a divide by two flip-flop coupled to both the phase frequency detector and the multiplier phase detector, the divide by two flip-flop conditioning a common input signal to both the phase frequency detector and the multiplier phase detector to a 50% duty cycle.

39. (New) The method of claim 38, wherein using the composite phase frequency detector includes using another divide by two flip-flop coupled to the phase frequency detector and a further divide by two flip flop coupled to the multiplier phase detector.

40. (New) The method of claim 38, wherein the multiplier phase detector includes a logic gate.

41. (New) The method of claim 40, wherein the logic gate includes an XOR gate.

42. (New) The method of claim 37, wherein the first frequency signal and the second frequency signal are characterized by a known integer ratio of frequency, phase or both frequency and phase.

43. (New) A digital data synchronization apparatus, comprising a synchronization circuit for synchronizing a frequency signal with a data signal and for generating a comparison signal,

wherein the synchronization circuit includes a composite phase frequency detector including a phase frequency detector, a multiplier phase detector coupled to the phase frequency detector and a divide by two flip-flop coupled to both the phase frequency detector and the multiplier phase detector, the divide by two flip-flop conditioning a common input signal to both the phase frequency detector and the multiplier phase detector to a 50% duty cycle.

44. (New) The digital-data synchronization apparatus of claim 43, further comprising another divide by two flip-flop coupled to the phase frequency detector and a further divide by two flip flop coupled to the multiplier phase detector.

45. (New) The digital-data synchronization apparatus of claim 43, wherein the multiplier phase detector includes a logic gate.

46. (New) The digital-data synchronization apparatus of claim 45, wherein the logic gate includes an XOR gate.

47. (New) A method of providing digital-data synchronization, comprising:

synchronizing a frequency signal with a data signal and generating a comparison signal using a synchronization circuit including a composite phase frequency detector having a phase frequency detector, a multiplier phase detector coupled to the phase frequency detector and a divide by two flip-flop coupled to both the phase frequency detector and the multiplier phase detector, and

conditioning a common input signal to both the phase frequency detector and the multiplier phase detector to a 50% duty cycle using the divide by two flip-flop.

48. (New) The method of claim 47, wherein using the composite phase frequency detector includes using another divide by two flip-flop coupled to the phase frequency detector and a further divide by two flip flop coupled to the multiplier phase detector.

49. (New) The method of claim 47, wherein the multiplier phase detector includes a logic gate.

50. (New) The method of claim 49, wherein the logic gate includes an XOR gate.

51. (New) A digital data synchronization apparatus, comprising:

a first synchronization circuit for synchronizing a first frequency signal with a first received data signal and for generating a first comparison signal; and

a second synchronization circuit for synchronizing a second frequency signal with a second received data signal and for generating a second comparison signal,

wherein the first frequency signal and the second frequency signal are characterized by a known integer ratio of frequency, phase or both frequency and phase.

52. (New) The digital-data synchronization apparatus according to claim 51, wherein the first frequency signal and the second frequency signal are derived from a common source that includes multiple components.

53. (New) The digital-data synchronization apparatus of claim 51, wherein at least one member selected from the group consisting of the first synchronization circuit and the second synchronization circuit includes a composite phase frequency detector including a phase frequency detector, a multiplier phase detector coupled to the phase frequency detector and a divide by two flip-flop coupled to both the phase frequency detector and the multiplier phase detector, the divide by two flip-flop conditioning a common input signal to both the phase frequency detector and the multiplier phase detector to a 50% duty cycle.

54. (New) The digital-data synchronization apparatus of claim 53, further comprising another divide by two flip-flop coupled to the phase frequency detector and a further divide by two flip flop coupled to the multiplier phase detector.

55. (New) The digital-data synchronization apparatus of claim 53, wherein the multiplier phase detector includes a logic gate.

56. (New) The digital-data synchronization apparatus of claim 55, wherein the logic gate includes an XOR gate.

57. (New) A method of providing digital-data synchronization, comprising:

synchronizing a first frequency signal with a first received data signal and generating a first comparison signal using a first synchronization circuit; and

synchronizing a second frequency signal with a second received data signal and generating a second comparison signal using a second synchronization circuit,

wherein the first frequency signal and the second frequency signal are characterized by a known integer ratio of frequency, phase or both frequency and phase.

58. (New) The method of claim 57, wherein at least one member selected from the group consisting of i) synchronizing the first frequency signal with the first received data signal and generating the first comparison signal using the first synchronization circuit and ii) synchronizing the second frequency signal with the second received data signal and generating the second comparison signal using the second synchronization circuit includes using a

composite phase frequency detector including a phase frequency detector, a multiplier phase detector coupled to the phase frequency detector and a divide by two flip-flop coupled to both the phase frequency detector and the multiplier phase detector, the divide by two flip-flop conditioning a common input signal to both the phase frequency detector and the multiplier phase detector to a 50% duty cycle.

59. (New) The method of claim 58, wherein at least one member selected from the group consisting synchronizing a the first frequency signal and synchronizing the second frequency signal includes using a composite phase frequency detector having another divide by two flip-flop coupled to the phase frequency detector and a further divide by two flip flop coupled to the multiplier phase detector.

60. (New) The method of claim 58, wherein the multiplier phase detector includes a logic gate.

61. (New) The method of claim 60, wherein the logic gate includes an XOR gate.